

In re Patent Application of:
GUINEA ET AL.
Serial No. **09/636,099**
Filing Date: **August 10, 2000**

REMARKS

Applicants would like to thank the Examiner for the thorough examination of the present application. The Abstract has been replaced with a shorter Abstract as requested by the Examiner. In addition, the typographical error on page 6 in the specification has been corrected as helpfully noted by the Examiner. In addition, an error noted by the Applicants on page 4 has also being corrected.

A certified copy of the priority application will be filed immediately upon receipt from the Applicants. The claims have been amended to correct the informalities as helpfully noted by the Examiner.

The Examiner also rejected the claims based upon the position that the specification is not enabling. Independent Claims 7, 13, 20 and 29 recite a second circuit for "determining based upon sampling whether two of the four local timing signals forming a pair of reference signals that are out of phase by $\frac{1}{2}$ period are advanced or delayed relative to the timing of the data flow, and for controlling the first circuit to delay or advance the four local timing signals based upon the pair of reference signals."

The Examiner references FIG. 3 in which timing signals **Q1**, **Q2** form a reference pair input into a first AND gate, and timing signals **Q3**, **Q4** form a reference pair input into a second AND gate. The Examiner notes that since the timing signals **Q1**, **Q2** illustrated in FIG. 4 have a phase difference of $\frac{1}{4}$ period, then the detector circuit illustrated in FIG. 3 is not enabled for forming a reference pair of timing signals having a phase difference of $\frac{1}{2}$ period, as recited in the independent claims.

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The Examiner's position is based on the pairing of timing signals **Q1**, **Q2** and timing signals **Q3**, **Q4**. As correctly noted by the Examiner, the timing signals **Q1**, **Q2** are out of phase by $\frac{1}{4}$, and the timing signals **Q3**, **Q4** are out of phase by $\frac{1}{4}$. The independent claims recite four local timing signals, but do not refer to a single pair of timing signals such as **Q1** and **Q2**, where they are out of phase by $\frac{1}{4}$.

The specification clearly states that the timing signals **Q1** and **Q3** are out of phase by $\frac{1}{2}$, and that the timing signals **Q2** and **Q4** are out of phase by $\frac{1}{2}$. This is also clearly illustrated by the timing diagram in FIG. 4. Page 5, lines 12-15 in the specification provides: "If the timing signal **Q1** is advanced or delayed, the timing signals **Q2-Q4** are also consequently advanced or delayed. Their delays relative to the signal **Q1** are kept constant."

In FIG. 3, the output **Q1'**, the negated output **Q2N'** of the flip-flops **FF1** and **FF2**, the output **Q3'**, and the negated output **Q4N'** of the flip-flops **FF3** and **FF4** are supplied to an AND-NOR-INVERTER logic gate **4**. The logic complement of the output of the logic gate **4** forms the signal +/- that is then supplied to the circuit **2**. The Applicants respectfully submit that the specification is enabling.

In view of the amendments to the claims and the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

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Respectfully submitted,



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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: MS AMENDMENT, COMMISSIONER FOR PATENTS, P.O. BOX 1450, ALEXANDRIA, VA 22313-1450, on this 7th day of January, 2005.

